Data Sheet

Alphanumeric display

RS stock number 585-191

The RS 1414 is a 4-digit alphanumeric display module complete with built-in CMOS driving circuitry. The on-board integrated circuit contains an ASCII decoder, multiplexer, memory and LED driver. Inputs are TTL compatible. Each digit consists of 16 bar-segments plus a decimal point segment for enhanced punctuation. A single 5V supply is the only power required by the module. The device is end-stackable enabling a display system to be built using any number of units, since each character in any device can be addressed independently and will continue to display the character last written until it is replaced by another.

The 1414 has a character height of 2.84mm and is ideal for hand held and portable instrumentation. The has a larger character height, 4.06mm, with additional blanking and cursor editing facilities.

Note: This device is manufactured using CMOS technology and should not be subjected to excessive levels of static charge in storage, handling or use, otherwise device failure is likely to occur. Please read this data sheet carefully particularly the section dealing with handling considerations.

Features

- Wide viewing angles ± 40°
- Close vertical row spacing: 20.3mm (0.8in)
- Rugged solid plastic encapsulated packages
- Fast access time: 280ns
- Built in memory
- Built in character generator
- Built in multiplex and LED drive circuitry
- Direct access to each digit independently and asynchronously
- TTL logic levels, 5V power
- End stackable packages.

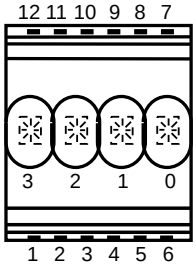
Absolute maximum ratings

Voltage (any pin with respect to ground) ___ -0.5 to +6Vdc
Operating temp. range _____ -40°C to +85°C
Storage temp. range _____ -40°C to +100°C

Input voltage (any pin)
under all conditions _____ $V_{IN} \leqslant V_{CC}$*
Relative humidity (non condensing) at 85°C _____ 85%
Soldering temp. _____ 260°C for 3 seconds
* See section on 'System design' considerations.

RS stock no. 585-191

TOP VIEW
1414



Product identification marks on this face

Pin Function

1. D5 Data input
2. D4 Data input
3. WR Write
4. A1 Digit select
5. AØ select
6. Vcc
7. Gnd
8. DØ Data input (LSB)
9. D1 Data input
10. D2 Data input
11. D3 Data input
12. D6 Data input (MSB)

2.84mm CHARACTERS ACTUAL SIZE

ALPHANUMERIC

Electrical and optical characteristics at 25°C

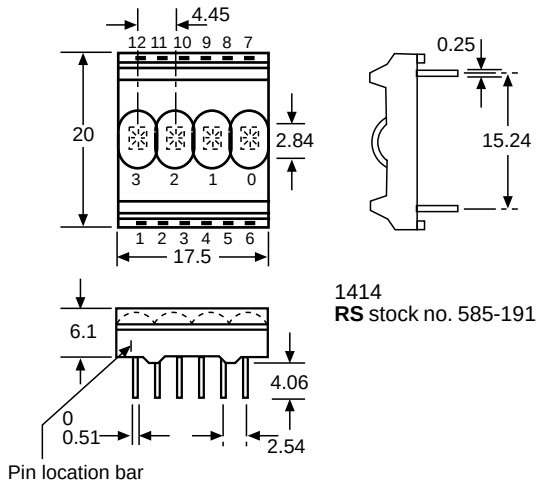
	Parameter	Conditions	Units	1414 Min.	1414 Typ.	1414 Max.
V_{CC}	Supply		V	4.5	5.0	5.5
I_{CC}	Supply current	All digits on (10 segs/dig.) V_{CC} = 5V	mA		50	65
		Display blank V_{IN} = 0, V_{CC} = 5V, WR = 5V	mA		1.0	2.7
		Cursor (60sec. max. duration)	mA			
V_{IL}	Input voltage - low (any input)	V_{CC} = 5V	V			0.8
V_{IH}	Input voltage - high (any input)	V_{CC} = 5V	V	2.0		*
I_{IL}	Input current - low (any input)	V_{IN} = 0.8V, V_{CC} = 5V	µA		60	160
	Luminous intensity	8 segments at 5V	mcd		0.55	
λpk	Spectral peak wavelength		nm		660	
θ	Off axis viewing angle	Note 1	degrees		±40°	

Note: 'Off axis viewing angle' is here defined as: 'The minimum angle in any direction from the normal to the display surface at which part any part of any segment in the display is not visible'.

* See Absolute maximum ratings.

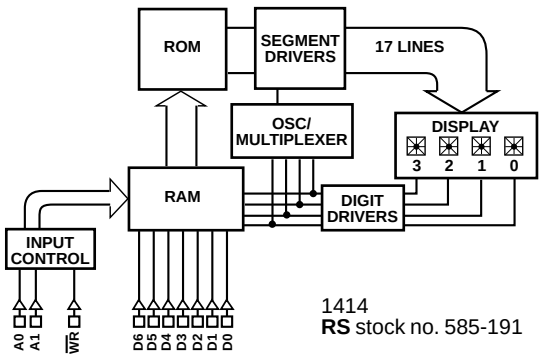
Caution: ESD (Electro-static-discharge) sensitive device. This CMOS device contains circuitry to protects the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that all input voltages constrained to the range V - ≤ V_{IN} ≤ V +, particularly during power up conditions.
Unused inputs made must be tied to an appropriate logic voltage level (either V+ or V-).

Figure 1 Dimensional details



1414
RS stock no. 585-191

Figure 2 Block diagram



1414
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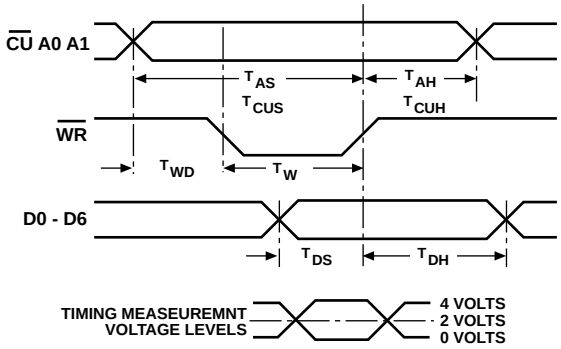
Table 1 Timing characteristic at 25°C

	Parameter	1414	Units
t_W	Write pulse	225	ns
t_{WD}	Write delay	30	ns
t_{DS}	Data set-up time	175	ns
t_{DH}	Data hold time	30	ns
t_{AS}	Address set-up time	250	ns
t_{AH}	Address hold time	30	ns
t_{CLR}	Clear time (see text)	-	ms
t_{CES}	Chip enable set up	-	ns
t_{CEH}	Chip enable hold	-	ns

Figure 3 Timing characteristics/write cycle waveforms



Electrical and mechanical description

General

The internal electronics on the RS intelligent displays eliminate all the traditional difficulties of using multi-digit light emitting displays (segment decoding, drivers and multiplexing). The intelligent display also provides internal memory for the four digits. This approach allows the user to asynchronously address one of four digits, and load new data without regard to the LED multiplex timing.

Figure 2 gives the block diagram of the 1414 display. The unit consist of four 17 segment monolithic LED die and a single CMOS integrated circuit chip. The LED die is a magnified to a height of 2.84mm (1414) by built-in lenses. The IC chip contains 17 segment drivers, four digit drivers, 64 character ROM, four word × 7 bit random access memory, oscillator for multiplexing, multiplex counter/decoder, address decoder, and miscellaneous control logic.

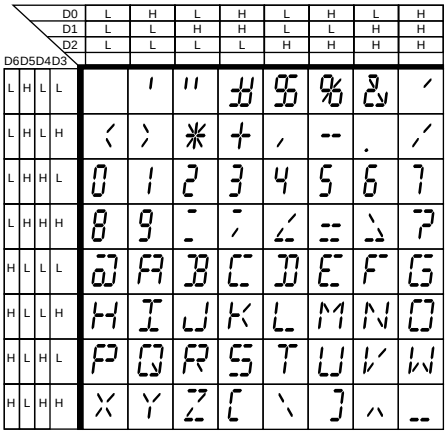
Packaging

Packaging consists of a plastic lens which also serves as an 'encapsulation shell' since it covers five of the six 'faces'. The assembled and tested substrate (ceramic or 'PTF' multilayer) is placed within the shell and the entire assembly is then filled with water-clear IC grade epoxy.

This yields a very rugged part which is quite impervious to moisture, shock and vibration. Although not 'hermetic', the device will easily withstand total immersion in water/detergent solutions.

Note: Solvents containing alcohol should not be used.

Figure 4 **Character set**



ALL OTHER INPUT CODES DISPLAY "BLANK"

Figure 5 **Digital address table**

A1	Aø	Digit
L	L	ø (Right)
L	H	1
H	L	2
H	H	3(Left)

Electrical inputs 1414

V_{CC}	Positive supply + 5 Volts
Gnd	Ground
D_0-D_6	Data lines The seven data input lines are designed to accept the first 64 ASCII characters. Refer to Figure 4 for character set.
A_0-A_1	Address lines The address determines the digit position to which the data will be written. Address order is right to left for positive-true logic.
$\overline{WR}$	Write (active low) Data and address to be loaded must be present and stable before and after the trailing edge or write (Refer to Figure 3 for timing information).

Operation

Multiplexed display systems sequentially read and display data from a memory device. In synchronous systems, control circuitry must compare the location of data to be read to the location or position of new data to be stored or displayed, ie. synchronise before a write can be done. This can be slow and cumbersome. Data entry in 'intelligent display' is asynchronous and may be done in any random order. Loading data is similar to writing into a RAM. Each digit has its own memory location and will display until replaced by another code.

The waveforms of Figure 3 demonstrate the relationship of the signals required to generate a write cycle. As can be seen from the waveforms, all signals are referenced from the rising or trailing edge of wire.

Data loading

Loading data into the display is straightforward. The desired data code (D_0-D_6) and digit address (A_0, A_1) are presented in parallel and held stable during a 'write' cycle. Data entry may be asynchronous and random (Digit 0 is defined as right hand digit with $A_1 = A_0 = 0$).

System interconnection

System interconnection is also straightforward. The least significant two address bits (A_0A_1) are normally connected to the like named inputs of all displays in the system. Data lines are connected to all displays directly and in parallel. For multiple 1414 systems an external 'one of N' decoder chip is usually used and the 'write' pulse connected to the enable of the decoder (Figure 6). A 3-to-8 line decoder multiplexer (74138) or a 4-to-16 line decoder/multiplexer (74154) are possible choices. All higher-order address bits (above A_1) become inputs to the decoder.

Figure 5 **Digital address table**

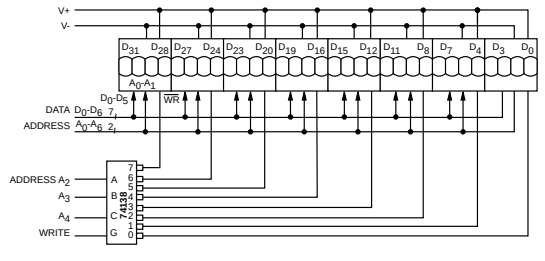
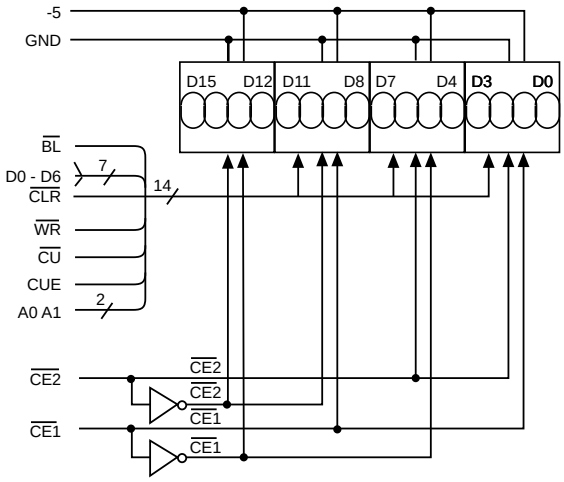


Figure 6 Typical interconnection for 32 digit system



Data loading tables

The following tables illustrate the operation of the above control functions. They are not 'truth tables' in that any one horizontal line is dependent on the preceding line.

Table 2 1414 loading data

WR	Address A_1	Address A_0	Data Input D6	D5	D4	D3	D2	D1	D0	Digit 3	Digit 2	Digit 1	Digit 0
H	X	X	X	X	X	X	X	X	X	No change	No change	No change	No change
L	L	L	H	L	L	L	L	L	H	No change	No change	No change	A
L	L	H	H	L	L	L	L	H	L	No change	No change	B	A
L	H	L	H	L	L	L	L	H	H	No change	C	B	A
L	H	H	H	L	L	L	H	L	L	D	C	B	A
L	L	L	H	L	L	L	H	L	H	D	C	B	E
L	H	L	H	L	L	H	L	H	H	D	K	B	E
L	-	-	-	-	-	-	-	-	-	See character set Figure 4			

X = Don't care

System design and construction

System design considerations

The practical circuit design (i.e. design of PCB, etc.) should be such that the voltage to any input must never exceed the power supply inputs (i.e. Gnd < V_{in} < V_{CC}). If these conditions are not met, then malfunction or at worst, device destruction can occur. The most common cause of this condition is circuit noise due to noise on the input leads and transient power supply changes.

Good circuit layout

The principles of good circuit layout are those for all logic circuitry, but the tolerance of MOS circuitry for deviations is much less than that of bipolar logic. The most important principle is to keep the lead length from the output of one device to the input of another as short as possible. This is to reduce the coupling effect between input signals.

Buffering The second most common deviation from good design practice is the use of parallel tracking. Avoid PCB design which allows an interconnection track to run parallel to another. This is particularly true if one of the tracks is a power bus when the fluctuations of power supply current can cause inductively coupled changes in the input track. Possibly the worst example of parallel tracking is the ribbon cable; it is physically neat and convenient, but can be electrically destructive for the MOS circuits.

It is often necessary, because of the very nature of the intelligent display, to use ribbon cable from the CPU board to the display assembly board. In those circumstances for cables over 30cm (12in), use a TTL buffer for each used input. This is especially true for noisy systems which have motors, relays etc. The buffers must be on the display end of the cable, thus maintaining a minimum distance between their outputs and the display inputs. Long cables can be a poor transmission line for speed pulses. Line drivers, line receivers, or Schmitt trigger gates may be required to shape pulses.

Voltage transients

It has become common practice to provide 0.01µF bypass capacitors liberally in digital systems. For intelligent displays, the emphasis is on adequate decoupling. Like other CMOS circuitry, the intelligent display controller chip has very low power consumption and the usual 0.01µF would be adequate were it not for the LEDs. The module itself can, in some conditions, use up to 100mA (multiplexed). In order to prevent power supply transients, capacitors with low inductance and high capacitance at high frequencies are required. This suggests a solid tantalum or ceramic disc for high frequency bypass. For larger displays distribute the bypass capacitors evenly, keeping capacitors as close to the power pins as possible. Do not rely on existing on-board decoupling: use a 10µF and 0.01µF for every 3 or 4 intelligent displays to decouple the displays themselves, at the displays.

Functional limitations Several parameters in this data sheet which may affect your design will be emphasised again. While these may not be destructive, they may affect reliability and/or functional operation.

1. The length of time all cursors may be lit should be 1 minute maximum.

2. The timing parameters for 25°C will increase with the increased temperature.
3. The timing parameters will increase with increased V_{CC}.

Handling considerations

Handling

The static voltages generated by friction with modern synthetic materials (ie. carpets, clothing, device carriers etc,) are often measured in thousands of volts. Although there is usually little energy in these static charges, to MOS circuitry that energy is sufficient to cause destruction if applied between circuit inputs. Input protection diodes can minimise the vulnerability of the circuits, but there is a limit to their protection capabilities. Under certain conditions, static charges can exceed that limit. The most effective protection is to avoid the generation of static charges. When they are inevitable, the charges must be prevented from coming in contact with the device pins.

1. Avoid touching the pins; handle the body only.
2. Keep the devices in anti-static tubes or conductive material when transporting.
3. Use conductive and grounded working area (conductive flooring, conductive work benches, individual wrist straps etc,).

Soldering Because of the plastic housing of the intelligent displays, it is necessary to control the solder temperature, soldering time and solder distance. A maximum of 260°C for 3 seconds at a distance of greater than $^1/_{16}$in is required. An additional requirement for wave soldering is that the intelligent display package temperature cannot exceed 70°C.

Cleaning The cleaning process for the intelligent displays is crucial to maintain the optical performance of the plastic housing. The solvent that **cannot** be used on the intelligent display product is alcohol. Alcohol will attack the lens material causing cracking, crazing and destruction of the clear optical properties of the lens.

In the suggested category are the chlorinated hydrocarbons (Acetone, 1.1.1. Trichloroethane, etc.) or Trichlorotrifluoroethane or warm deionised water.

Caution: Do not specify a solvent without first finding the chemical composition. Some manufacturers use some form of alcohol as an additive, so beware.

Interfacing the 1414

The general and straightforward interface circuit shown in Figure 6 can easily interface to microprocessor systems or any other systems which can provide the seven data lines, appropriate address and control lines.

The 1414 does not have a chip enable input. Therefore, each 1414 in a system requires its write pulse to be gated with appropriate address signals. Figure 7a shows the use of a 74154 decoder (4 line to 16 line) for up to a 64 character display. Using the G1 input for display select (address select in a memory mapped system) and the G2 input to gate the write signal. Another approach (Figures 7b and 7c), which minimises logic for a 16 or 32 digit display takes advantage of decoding scheme of the 7442 decoder.

Parallel I/O

The parallel I/O device of a microprocessor can easily be connected to the circuit in Figure 8. One eight bit output port can provide the seven input data bits. Another eight bit output port can contain the address and control signals required by the display.

Figure 7 **Gating wire impulse**

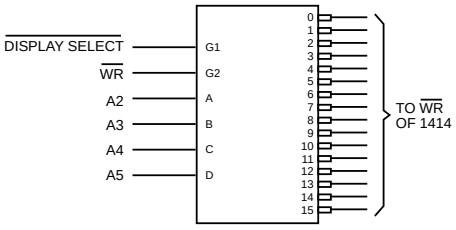


Figure 8a

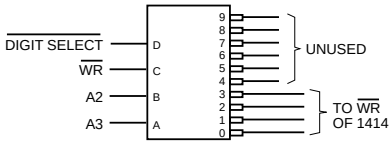


Figure 8b

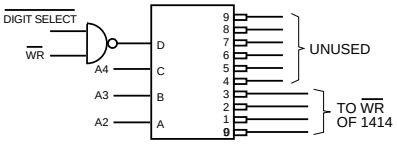


Figure 8c

Figure 8 16 digit parallel I/O system